THE PAPUA NEW GUINEA UNIVERSITY OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND COMMUNICATIONS ENGINEERING

SECOND SEMESTER EXAMINATION – 2021

EE221: DIGITAL LOGIC SYSTEMS

BEEL2, BSAP2 & BEBE2

TIME ALLOWED: 3 HOURS

INFORMATION FOR STUDENTS:

1. You have **TEN [10] MINUTES** to read through the paper. You must not begin writing during this time until you are told to.
2. Answer ALL **SIX QUESTIONS**. Attend to **all the Examination Questions** in **any order**.
3. All answers must be written in the **ANSWER BOOK** supplied.
4. Make sure that you have a physical data sheet at the final page of the Exam Paper.
5. **COMPLETE THE DETAILS REQUIRED ON THE FRONT COVER OF YOUR ANSWER BOOKLET – DO THIS NOW!**
6. Only the drawing instruments and the calculators are permitted on your desk. Text books and notebooks are **NOT** permitted.
7. If you are found cheating in the Examination, the penalties specified by the University shall apply.
8. **TURN OFF** all **Mobile Phones** and place them on the floor under your seat before the start of Examination.

"GOOD LUCK"

Question 1: [10 Marks]

The Exxon-Mobil PNG LNG in their chemical processing plant uses a microcomputer to monitor the temperature and pressure of four chemical tanks, as shown in *Figure 1*. Whenever a temperature or a pressure exceeds the danger limit, an internal tank sensor applies a 1 (High) to its corresponding output to the microcomputer. If all conditions are OK, then all outputs are 0.

A) If the microcomputer reads the binary string $0011\ 1110_2$, what problem exist? [**2 marks**]
B) What problems exist if the microcomputer is reading $C9_{16}$ (C9 Hex)? [**2 marks**]
C) What hexadecimal number is read by the microcomputer if the temperature and pressure in tanks A, B and D are HIGH? [**2 marks**]
D) What is the binary number read by the computer if temperature in tank A is HIGH and both temperature and pressure in tank B are HIGH? [**2 marks**]
E) In another area of the plant, only three tanks (A, B, and C) have to be monitored. What octal number is read if tank B has a HIGH temperature and pressure? [**2 marks**]

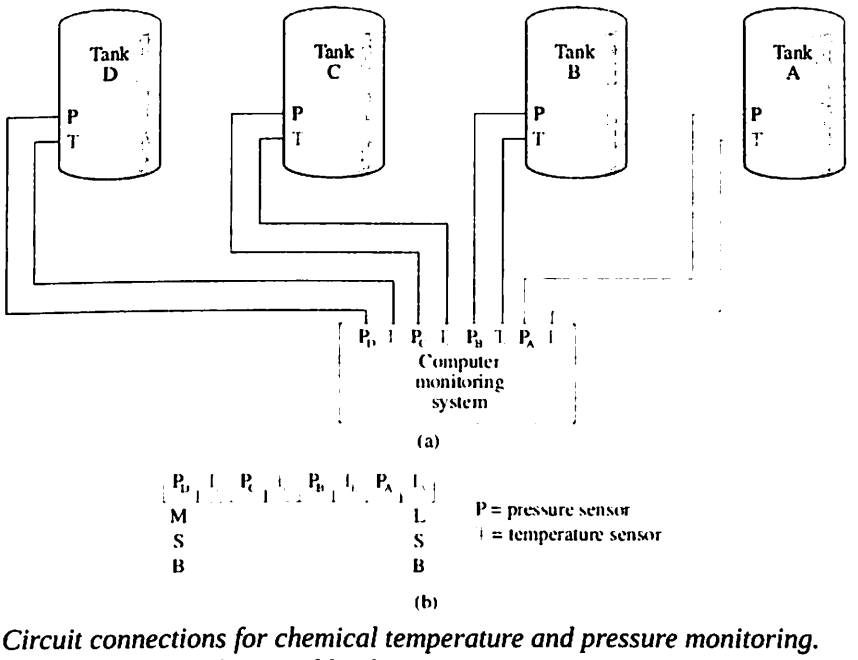


Figure 1. (a) Circuit connections for chemical temperature and pressure monitoring.
(b) Layout of binary data read by the computer monitoring system.

Question 2: [10 Marks]

A) Convert 1011.0011_2 binary number to its equivalent decimal number. [**2 marks**]

B) Convert 115.243_8 octal number into it's equivalent decimal number. [**2 marks**]

C) Perform the BCD addition by first converting the decimal numbers 78_{10} and 68_{10} into its equivalent BCD. [**2 marks**]

D) Perform the binary subtraction of 8_{10} from 11_{10}. [**2 marks**]

E) Perform the Hexadecimal addition of $16CF_{16}$ into $CA3F_{16}$. [**2 marks**]

Question 3: [10 Marks]

1. Inside a certain Liquefied Petroleum Gas (LPG) storage plant, three tanks (*A, B, C*) are equipped with liquid level switches. The level sensor in each tank produces a HIGH voltage only when the level of

LPG in the tank drops below a specified point. You are required to design a combinational logical circuit that monitors the LPG level that activates an alarm (*X)* when the level in *any two or more* of the tank drops below the specified point.

A) Derive the Truth Table that describes the logical design problem above. [**1 mark**]

Table1. Truth Table

A	B	C	X (*Alarm*)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

B) From the Truth Table (Table 1) in (A), derive the general Boolean expression for the activated alarm output. [**1 mark**]

C) From the Truth Table in (A) and/or Boolean expression in (B), simplify to its simplest equivalent expression

I. using K-Mapping technique. [**1 mark**]

II. using DeMorgan's theorem and algebraic reduction method(s). [**1 mark**]

D) Draw the logic circuit diagram of the simplified expression in (C). [**1 mark**]

2. *Figure 2* shows an analog-to-digital converter circuit that is used to monitor the DC voltage of a 12-V storage battery of an airborne drone. The converters output is a 4-bit binary number, *ABCD*, corresponding to the battery voltage of 1-V with *A* as the MSB. The converters output are fed to a logic circuit that is to produce a HIGH output as long as the binary value is grater than $0110_2 = 6_{10}$; that is the battery voltage is garter than 6-V.

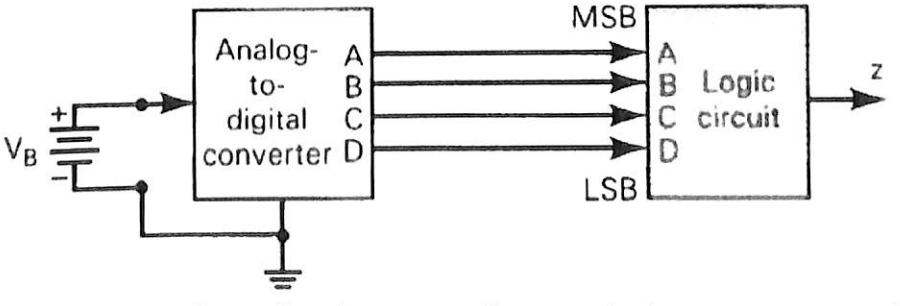


Figure 2. Analog-to-digital converter of a 12-V 4-bit battery monitoring schematic.

A) Derive the Truth Table that describes the logical design problem above. [**1 mark**]

Table 2. Truth Table

	A	B	C	D	z
(0)	0	0	0	0	
(1)	0	0	0	1	
(2)	0	0	1	0	
(3)	0	0	1	1	
(4)	0	1	0	0	
(5)	0	1	0	1	
(6)	0	1	1	0	
(7)	0	1	1	1	
(8)	1	0	0	0	
(9)	1	0	0	1	
(10)	1	0	1	0	
(11)	1	0	1	1	
(12)	1	1	0	0	
(13)	1	1	0	1	
(14)	1	1	1	0	
(15)	1	1	1	1	

B) From the Truth Table in (A), derive the general Boolean expression for the activated alarm outputs. [**1 mark**]

C) From the Truth Table in (A) and/or Boolean expression in (B), simplify to its simplest equivalent expression using K-Mapping technique. [**2 marks**]

D) Draw the logic circuit diagram of the simplified expression in (C). [**1 mark**]

Question 4: [10 Marks]

An XOR gate can have more than one implementation. That is constructing it using the basic gates or combining only the universal gates. The expression of an XOR gate with inputs *A* and *B* and output *X* is;

$$X = (A + B) \cdot \overline{(A \cdot B)} = A\,\overline{B} + \overline{A}\,B$$

which is then represented as

$$X = A \oplus B$$

The equivalent circuit diagram for the XOR using OR gate, AND and NAND gate is given in *Figure 3*.

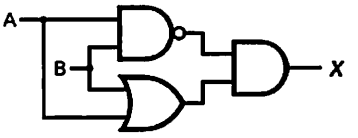
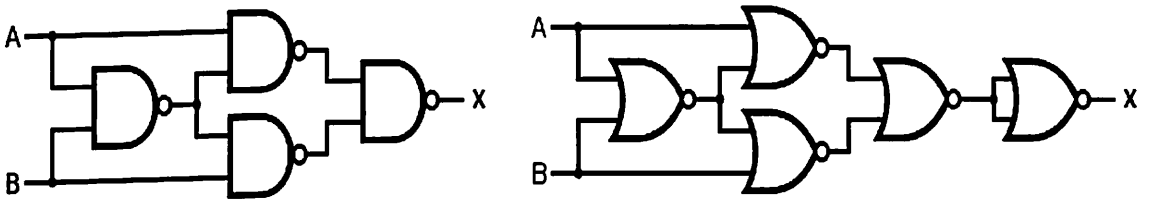


Figure 3: XOR gate

A) Prove by using DeMorgan's theorems and Boolean laws that XOR equivalent circuit implementations in *Figure 4 (a)* and *(b)* are also XOR gates. **[6 marks]**



(a) XOR by NAND Implementation *(b)* XOR by NOR Implementation

Figure 4: XOR: (a) XOR by NAND and (b) XOR by NOR

B) Draw the logic circuit that fits this Boolean algebraic expression. **[2 marks]**

$$X = \overline{[\overline{A} + \overline{B} + C]} \oplus BD$$

C) Write down the Boolean expression of the circuit given in *Figure 5* and simplify using DeMorgan's theorems and Boolean laws. The algebraic variables are; *M*, *N* and *Q* as inputs and the output is *X*. **[2 marks]**

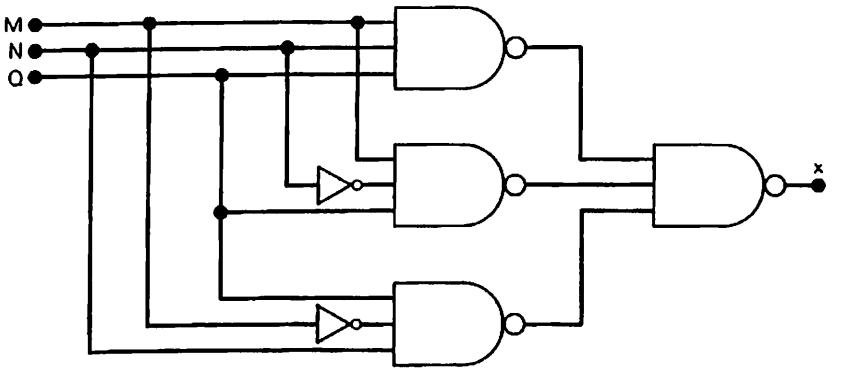


Figure 5. Combinational logic circuit

Question 5 [10 Marks]

1. The internal circuitry of a positive-going-transition (PGT) edge triggered J-K flip-flop is show in *Figure 6* below.

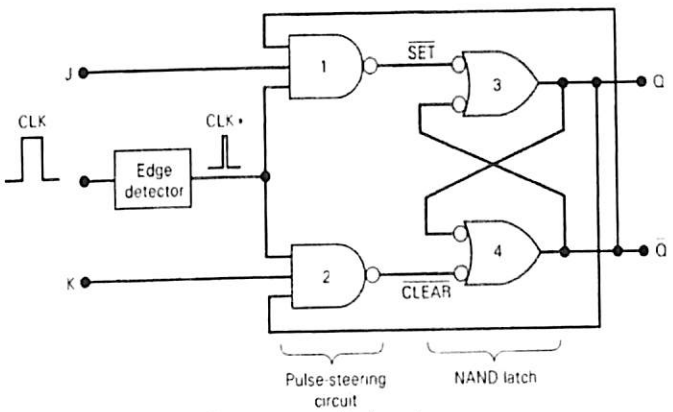


Figure 6. J-K flip-flop internal circuitry.

A) Determine the *Q* output Function Table of the edge-triggered J-K flip-flop in *Figure 6* . [**2 marks**]

Table 3: J-K flip-flop function table

J	K	CLK	Q
0	0	↑	
1	0	↑	
0	1	↑	
1	1	↑	

B) Complete the waveform of the *Q* output of the *Figure 7* below based on the derived Function Table in *Table 3*. [**2 marks**]

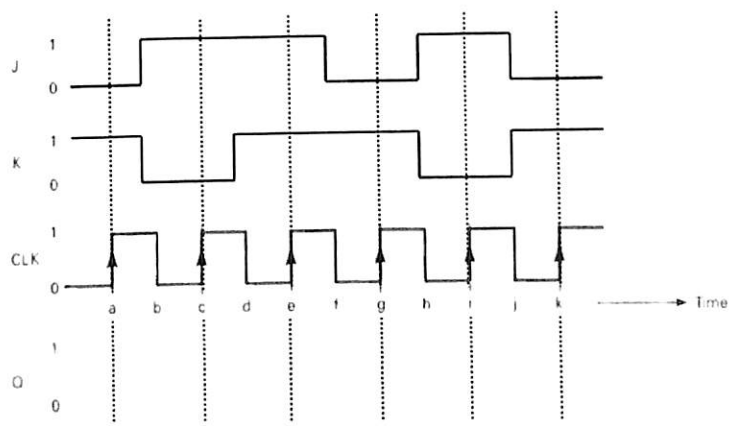
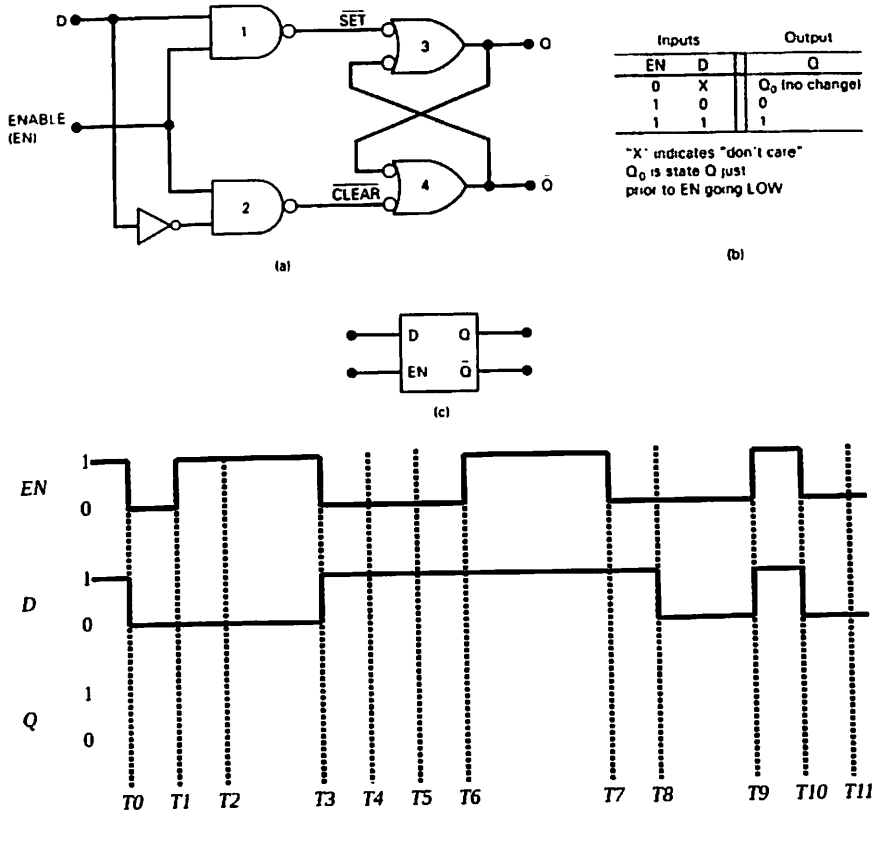


Figure 7. J-K flip-flop waveform(s).

2. *Figure 8 (a), (b)* and *(c)* shows the internal structure, truth table and symbol respectively of an edge-triggered transparent D latch. Draw the Q output waveform of *Figure 8 (d).* **[2 marks]**



(d)

Figure 8. Transparent D latch: (a) structure, (b) truth table, (c) symbol, (d) waveform.

3. *Figure 9 (a), (b)* and *(c)* shows the symbol, Function Table and the internal structure of a gated S-R flip flop. Note that the S_x and R_x lines are the original Set and Reset inputs, however, with the addition of the AND gates, these S_x and R_x lines will be kept LOW-LOW (Hold condition) as long as the Gate Enable is LOW. The flip-flop will operate normally while the Gate Enable is HIGH as can be seen in the Function table and also indicated in the internal stricture diagram.

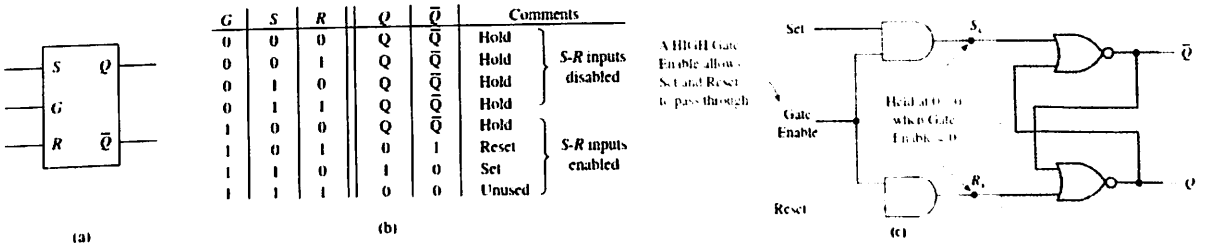
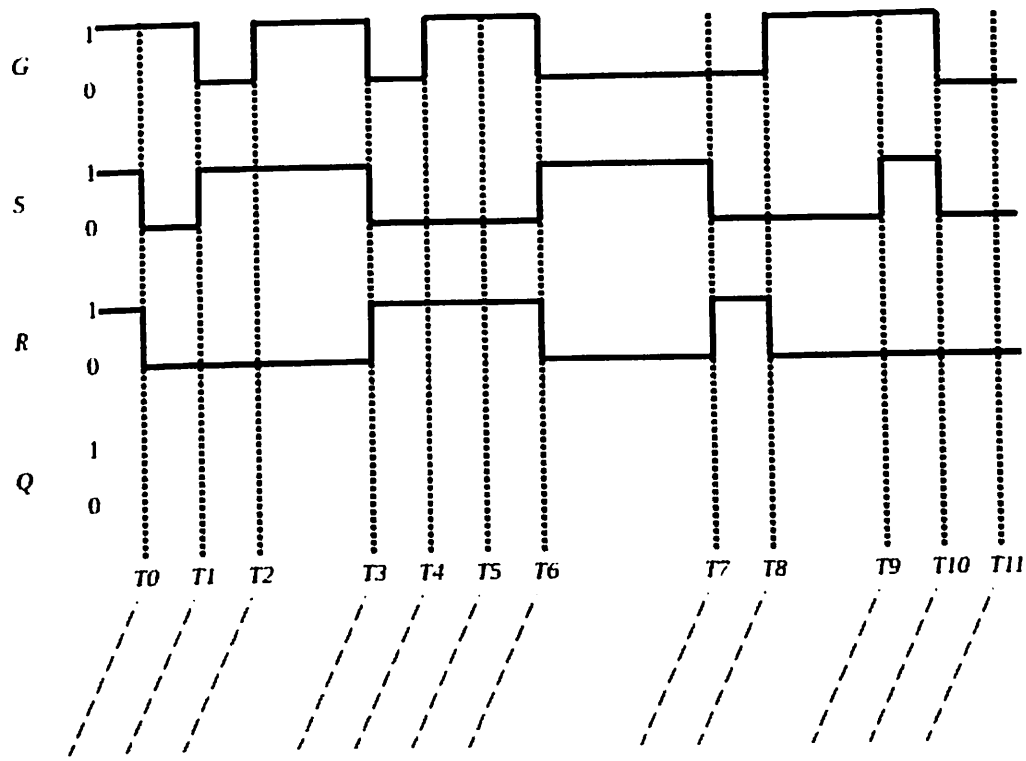


Figure 9. Gated S-R flip-flop: (a) Symbol, (b) Function table, (c) Structure,

Feed the *G*, *S*, and *R* inputs in *Figure 9 (d)* below of the waveform diagram into the gated *S-R* flip-flop in *Figure 9 (c)*, and utilizing the input conditions of the Function table in *Figure 9 (b)*, sketch the output waveform of *Q* at *Figure 9 (d)*, and comment the flip-flop functions under *Q* output waveform. **[4 marks]**



(d)

Cont ... Figure 9. Gated S-R flip-flop: (d) waveform.

Question 6 [10 Marks]

1. *Figure 10 (a)* and *(b)* shows a J-K flip-flop 3-bit counter circuit and its state change waveform respectively. [*Note: J = K = 1 (toggles)*].

   A) Why is Clocked J-K flip-flop used to implement counters and not D or S-R flip-flops? **[1 mark]**

   B) Calculate the MOD number of the 3-bit counter circuit in *Figure 10 (a)*. **[1 mark]**

   C) Determine the frequency at the output of the last FF (Q_2) when the input clock frequency is 1 MHz. **[1 mark]**

$$Frequency(Q) = \frac{Clock\ frequency}{Mode\ number}$$

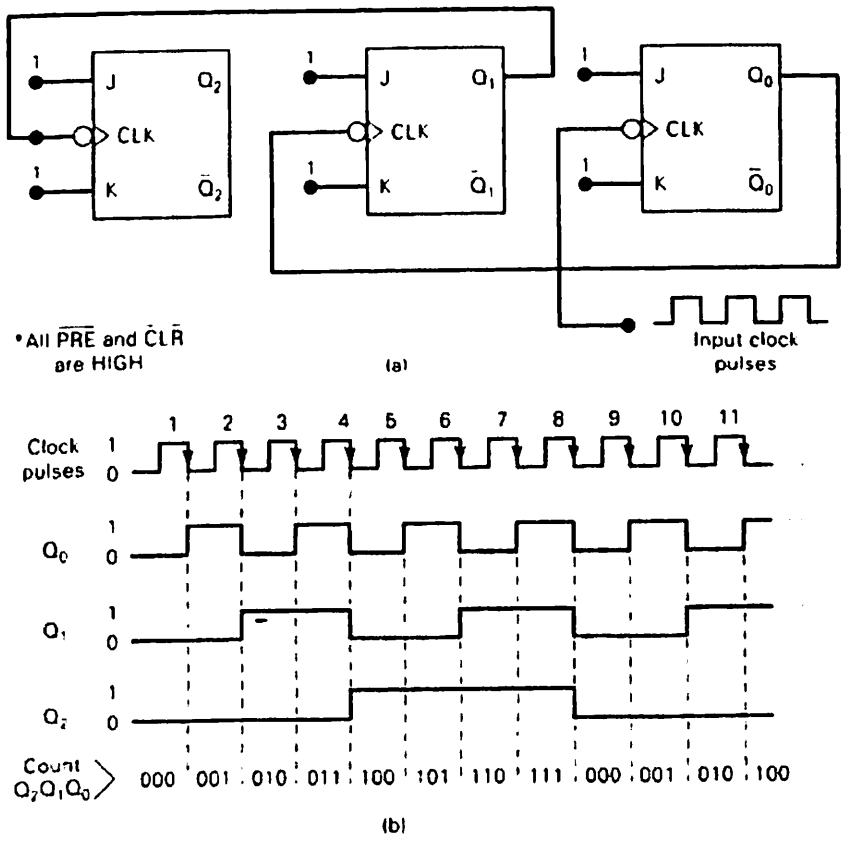


Figure 10. J-K flip-flop wired as a three-bit (3 flip flops) binary counter: (a) 3-bit counter circuit, (b) counter state change waveform.

D) Redraw the J-K flip-flop counter circuit in *Figure 10 (a)* containing six FFs, (i.e. Q_5,Q_4,Q_3,Q_2,Q_1,Q_0). **[1 mark]**

E) Calculate the MOD number of the counter circuit drawn in (D). **[1 mark]**

F) Determine the frequency at the output of the last FF (Q_5) of the counter circuit drawn in (D) when the input clock frequency is 1 MHz. **[1 mark]**

G) What is the range of counting states of counter drawn in (D)? **[1 mark]**

H) Assuming a starting sate (count) of 000000. What will be the counter's state after 129 clock pulses of the counter circuit drawn in (D)? **[1 mark]**

I) Another way to illustrate the states of flip-flops change with each applied clock pulse is by using a **state transition diagram** (STD). *Figure 11* shows the incomplete STD of the J-K counter circuit of *Figure 10 (a)*.

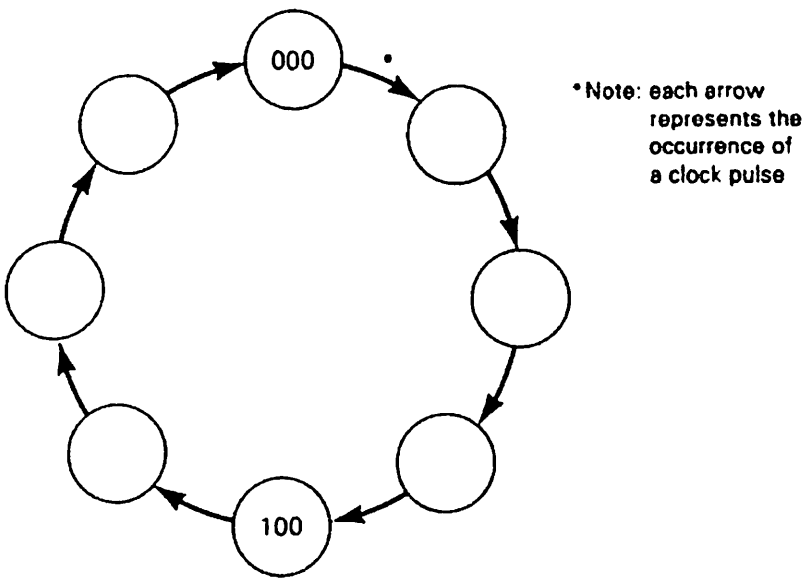


Figure 11. J-K flip-flop state transition diagram (STD) of 3-bit J-K flip-flop counter.

Note that at the start, $Q_2 = Q_1 = Q_0 = 0$ (000). Complete the empty states of the STD in *Figure 11*. [2 marks]

Exam Data Sheet

TABLE 2	Boolean Laws and Rules for the Reduction of Combinational Logic Circuits
Laws	
1	$A + B = B + A$ $AB = BA$
2	$A + (B + C) = (A + B) + C$ $A(BC) = (AB)C$
3	$A(B + C) = AB + AC$ $(A + B)(C + D) = AC + AD + BC + BD$
Rules	
1	$A \cdot 0 = 0$
2	$A \cdot 1 = A$
3	$A + 0 = A$
4	$A + 1 = 1$
5	$A \cdot A = A$
6	$A + A = A$
7	$A \cdot \overline{A} = 0$
8	$A + \overline{A} = 1$
9	$\overline{\overline{A}} = A$
10 (a)	$A + \overline{A}B = A + B$
(b)	$\overline{A} + AB = \overline{A} + B$

In the form of an equation, **De Morgan's theorem** is stated as follows:

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

Also, for three or more variables,

$$\overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$$

$$\overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$$