THE PAPUA NEW GUINEA UNIVERSITY OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND COMMUNICATIONS ENGINEERING

SECOND SEMESTER EXAMINATION – 2022

EE221: DIGITAL LOGIC SYSTEMS

BEEL2, BSAP2, BEBE2

TIME ALLOWED: 3 HOURS

INFORMATION FOR STUDENTS:

1. You have **TEN [10] MINUTES** to read through the paper. You must not begin writing during this time until you are told to.
2. Answer ALL **SIX QUESTIONS**. Attend to **all the Examination Questions** in **any order**.
3. All Answers must be written in the **ANSWER BOOK** supplied.
4. **COMPLETE THE DETAILS REQUIRED ON THE FRONT COVER OF YOUR ANSWER BOOKLET – DO THIS NOW!**
5. Only the drawing instruments and the calculators are permitted on your desk. Text books and notebooks and any electronic readers are **NOT** permitted.
6. If you are found cheating in the Examination, the penalties specified by the University shall apply.
7. **TURN OFF** all **Mobile Phones** and place them on the floor under your seat before the start of Examination.

"GOOD LUCK"

Question 1: [10 marks]

A. Convert binary 1101.101 to its equivalent decimal number. [**1 mark**]

B. Perform the following arithmetic operations;

i. Add $4A_{16}$ with $3B_{16}$ [**1 mark**]

ii. Subtract decimal 16 from 12 in binary. [**1 mark**]

C. Name the two major types of logic circuits used in digital logic designs. [**2 marks**]

D. The Exxon-Mobil PNG LNG in their chemical processing plant uses a microcomputer to monitor the temperature and pressure of four chemical tanks, as in Figure 1. Whenever a temperature or a pressure exceeds the danger limit, an internal tank sensor applies a 1 (High) to its corresponding output to the microcomputer. If all conditions are OK, then all outputs are 0 (Low).

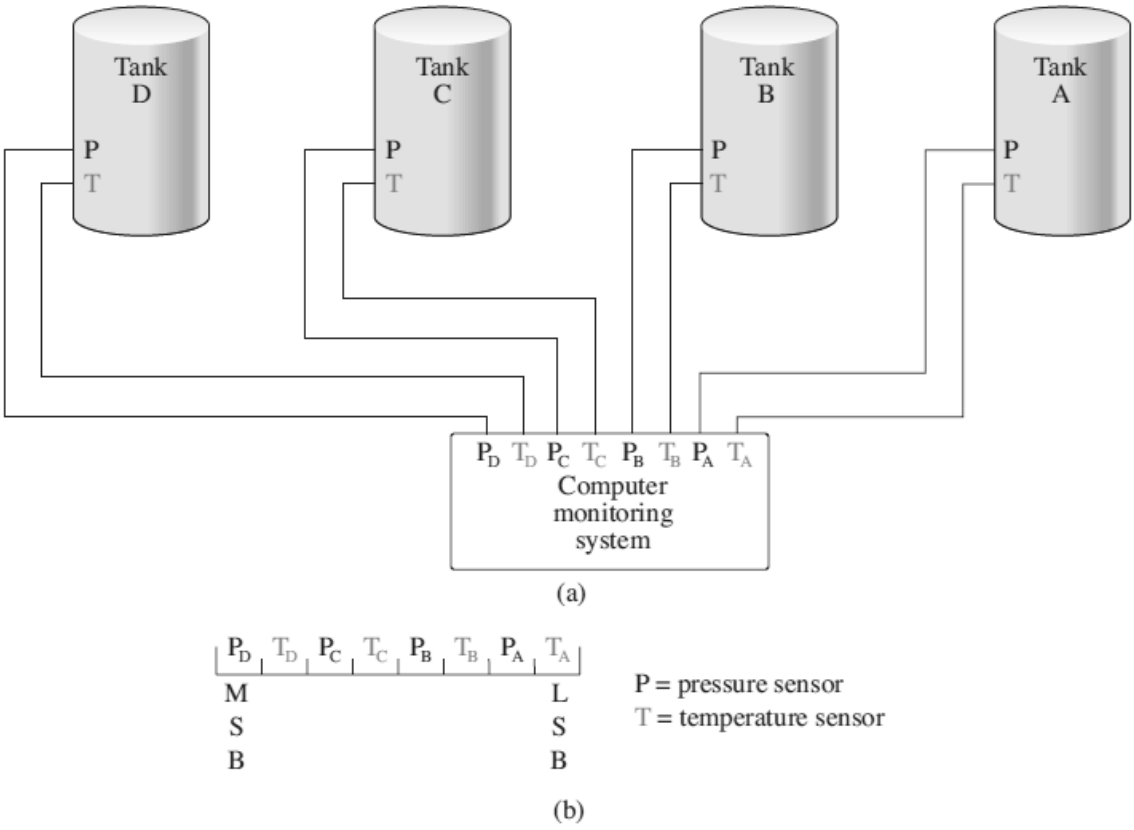


Figure 1. (a) Circuit connections for chemical temperature and pressure monitoring. (b) Layout of binary data read by the computer monitoring system.

i. If the microcomputer reads the binary string 0011 11102, what problem(s) exist? [**1 mark**]
ii. What problem(s) exist if the microcomputer is reading $A2_{16}$ (A2 Hex)? [**1 mark**]
iii. What hexadecimal number is read by the microcomputer if the temperature and pressure in tanks A and C are HIGH? [**1 mark**]
iv. What is the binary number read by the computer if temperature in tank B is HIGH and both temperature and pressure in tank D are HIGH? [**1 mark**]
v. In another area of the plant, only three tanks (A, B, and C) have to be monitored. What hexadecimal number is read if tank A has a HIGH temperature and pressure? [**1 mark**]

Question 2: [10 marks]

A. Inside a certain Liquid Petroleum Gas (LPG) storage plant, each three tanks (*A*, *B*, C) are equipped with liquid level sensors. The level sensor in each tank produces a HIGH level only when the level of LPG in the tank drops below a specified point. Design a logical circuit that monitors the LPG level that activates an alarm (*X)* when the level in *any two or more* of the tank drops below the specified point.

i. Derive the Truth Table of the tank level monitoring. [**2 marks**]

A	B	C	*X* (*Alarm*)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

ii. From the Truth Table in *i*, derive the general Boolean expression for the activated alarm output. [**1 mark**]

iii. From the Truth Table in *i* and/or Boolean expression in *ii*, use K-map and/or algebraic reduction method(s) (*use only one method*) and simplify to its simplest equivalent expression. [**2 marks]**

iv. Draw the logic circuit diagram of the simplified expression in *iii*. [**1 mark**]

B. Consider the combinational logic circuit shown in Figure 1. [**4 marks**]

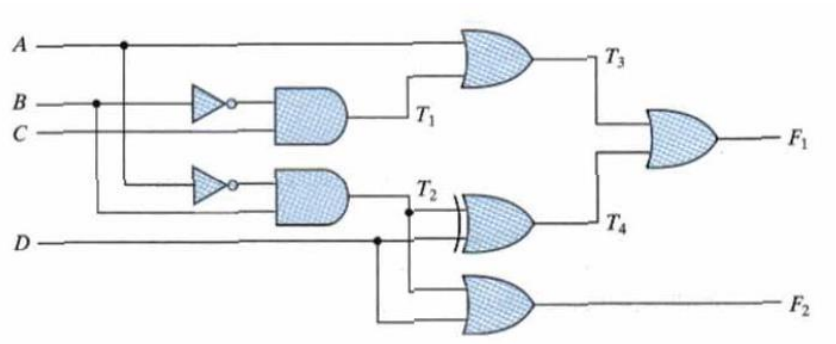


Figure 2: Combinational logic circuit.

Derive the Boolean expressions for the two outputs (F_1 and F_2).

i. F_1
ii. F_2

Question 3: [10 marks]

A. Applying algebraic reasoning and De'Morgans theorems, for each circuit shown in Figure 3, prove mathematically if its output provides the **Ex-OR** function, the **Ex-NOR** function, or **neither**. [**3 marks**]

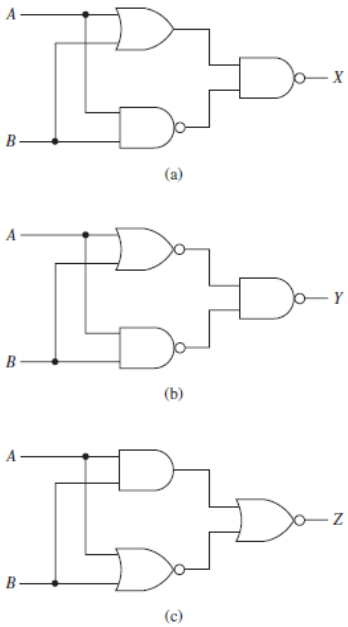
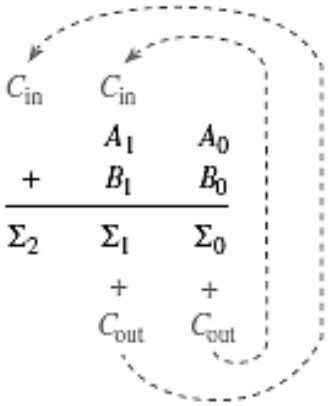


Figure 3: (a), (b) and (c).

B. Figure 4 shows the summation operation and its characteristics truth table. It shows the full adder operation where A and B are the two inputs and additional C_{in} is the carry input from the previous addition of the least significant bit which was generated by the C_{out} (carry out). The $\sum_1$ is the sum output.



Full adder Truth Table

A_1	B_1	C_{in}	Σ_1	C_{out}
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Figure 4: Addition in the more significant columns requires including C_{in} with $A_1 + B_1$.

I. Completely fill in the Truth table. [**1 mark**]

II. Determine the simplified algebraic expression of the sum ($\sum_1$) by;

i. From the Truth table in (I), derive the sum of product (SOP) terms of the $\sum_1$. [**1 mark**]

ii. Use any or both of the logic circuit reduction techniques and simplify the SOP of the $\sum_1$ in (i)? [**1 mark**]

III. Determine the simplified algebraic expression of the carry out (C_{out}) by;
   i. From the Truth table in (I), derive the sum of product (SOP) terms of the C_{out}. [**1 mark**]
   ii. Use any or both of the logic circuit reduction techniques and simplify the SOP of the C_{out} in (i)? [**1 mark**]

IV. Finally, using the reduced logic expressions in (II) and (III) above, draw the combined and simplified logic circuit of the full adder. [**1 mark**]

V. Name an advantage of reducing combinational circuits to its simplest. [**1 mark**]

Question 4: [10 marks]

A. The internal circuitry of a positive-going-transition (PGT) edge triggered J-K flip-flop is show in Figure 5 below.

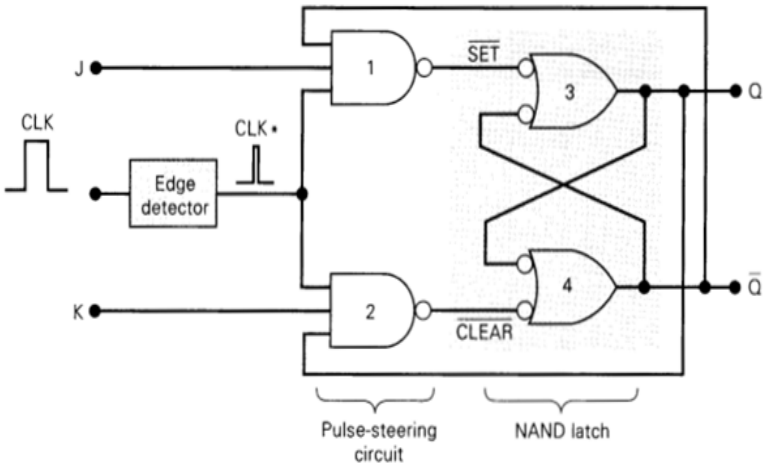


Figure 5. J-K Flip-flop internal circuitry.

I. Determine the *Q* output function table of the clocked J-K flip-flop in Figure 5 above. [**1 mark**]

Table 1: J-K flip-flop function table

J	K	CLK	Q
0	0	↑	
1	0	↑	
0	1	↑	
1	1	↑	

II. Complete the waveform of the *Q* output of the Figure 6 below based on the derived function table in *Table 1* and *Figure 5* above. [**1 mark**]

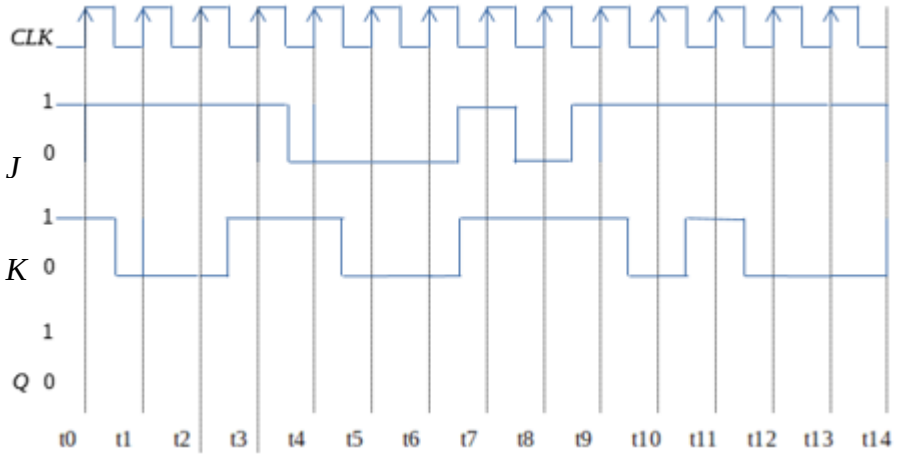


Figure 6. J-K Flip-flop internal circuitry.

B. Figure 7 (a), (b) and (c) shows the internal structure, truth table and symbol respectively of a level-triggered transparent D latch. Draw the *Q* output waveform of Figure 3 (d). [**2 marks**]

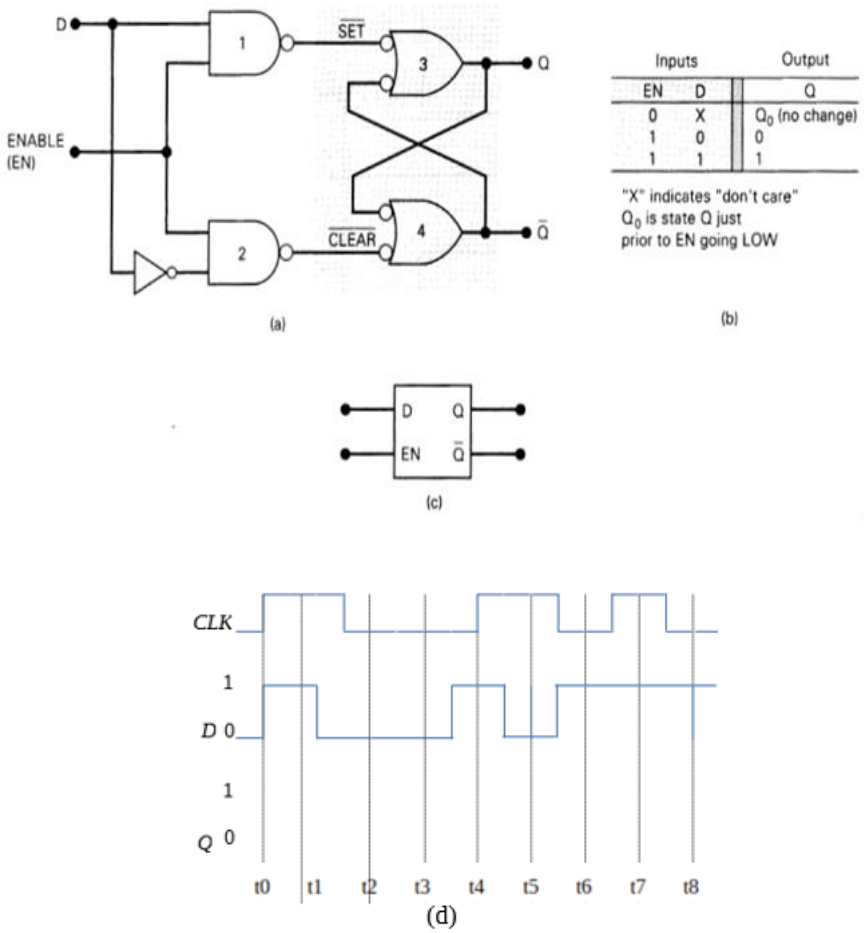


Figure 7. Transparent D latch: (a) structure, (b) truth table, (c) symbol, (d) waveform.

B. Figure 8 (a), (b) and (c) shows the symbol, function table and the internal structure of a gated S-R flip flop. Note that the *S* and *R* lines are the original Set and Reset inputs, however, with the addition of the AND gates, these *S* and *R* lines will be kept LOW-LOW (Hold condition) as

long as the Gate Enable is LOW. The flip-flop will operate normally while the Gate Enable is HIGH as can be seen in the function table and also indicated in the internal structure diagram.

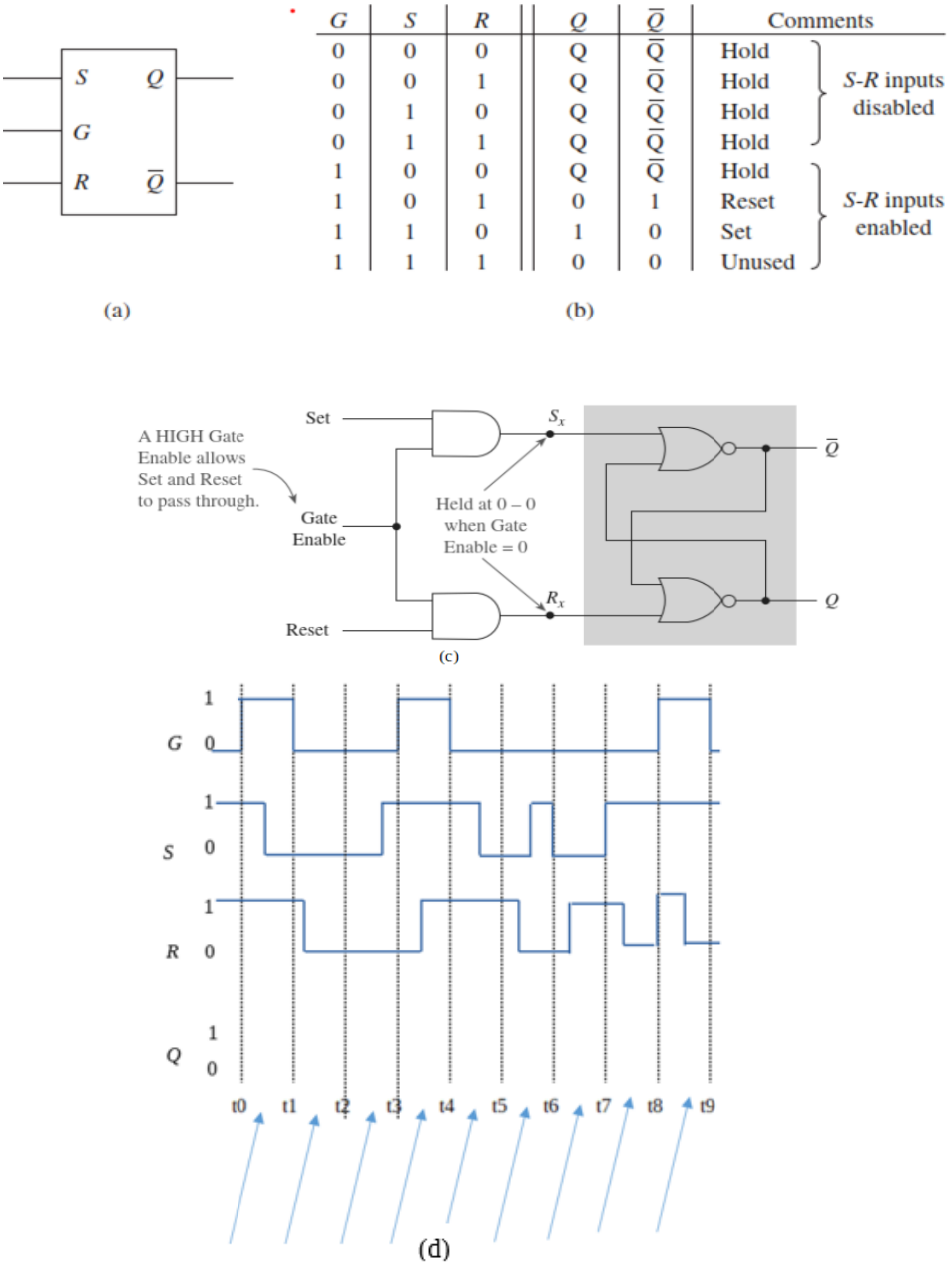


Figure 8. Gated S-R flip-flop: (a) symbol, (b) function table, (c) internal structure, (d) waveform

Feed the *G*, *S*, and *R* inputs into *Figure 8 (d)* of the waveform diagram into the gated *S-R* flip-flop in *Figure 8 (c)* by utilizing the input conditions of the function table in *Figure 8 (b)*.

Question 5: [10 marks]

Block diagram of Figure 9 shows a Ripple MOD-32 up counter. The counter is implemented using five clocked J-K Flip-Flops; [Note: J = K = 1].

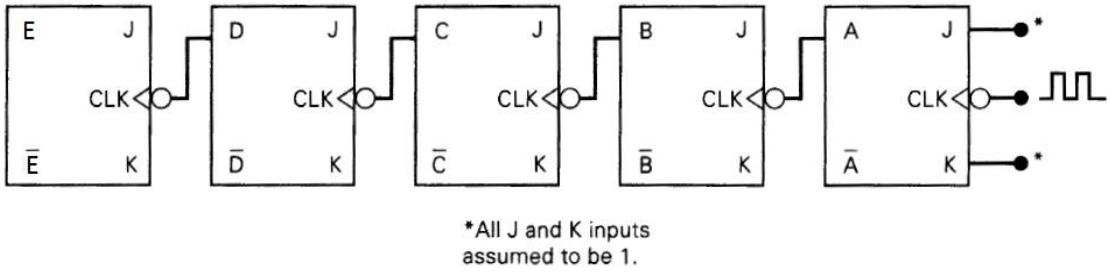


Figure 9: MOD-32 ripple up counter.

a. Why is Clocked JK Flip-Flop used to implement counters and not D or S-R flip-flops? [**1 mark**]
b. If Clocked J-K Flip – Flop with Asynchronous inputs are used to implement the MOD-32 up counter circuit as shown above, what must be done to the asynchronous inputs. [**2 marks**]
c. Sketch a MOD 32 down counter circuit based on arrangement given in *Figure 9* by using Clocked J-K Flip – Flop with Asynchronous inputs. [**3 marks**]
d. Ripple Counters with MOD Number $<2^N$, where N is the number of Flip Flops. Sketch the circuit diagram of a Ripple MOD-27 UP COUNTER using five Clocked J-K F-F with Asynchronous inputs and NAND gates. [**4 marks**]

Question 6: [10 marks]

I. The serial in serial out (SISO) **synchronous shift register** of a 3-bit data transfer circuit can be built using any flip-flop. Assuming a PGT shift pulse, D_2, D_1 and D_0 as the data input and Q_2, Q_1 and Q_0 as the data outputs:

i. Draw the block diagram with the correct number of flip-flops with input/output labeling. [**2 marks**]

ii. Assuming the **synchronous shift register** you drawn in (i) has the binary number 101 to be transferred when shift pulse is applied. Complete the shifting of the 3-bits in Truth table below. The initial state is done for you assuming 000. [**2 marks**]

Clk	D	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0	0
1	D_0 -> 1				
2	D_1 ->0				
3	D_2 -> 1				
4					
5					

II. The block diagram of the serial in parallel out (SIPO) **synchronous shift register** of a 4-bit data transfer circuit can be developed using any of the flip-flop. Assuming a NGT shift pulse, D_3, D_2, D_1 and D_0 as the data inputs and Q_3, Q_2, Q_1 and Q_0 as the data output:

i. Draw the block diagram with the correct number of flip-flops with input/output labeling. [**2 marks**]

ii. Assuming the **synchronous shift register** you drawn in (i) has the binary number 1110 to be transferred when shift pulse is applied. Complete the shifting of the 4-bits in Truth table below. The initial state is done for you assuming 0000. [**2 marks**]

Clk	D	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0	0
1	D_0 -> 0				
2	D_1 ->1				
3	D_2 -> 1				
4	D_3 -> 1				
5					

iii. Represent the 4-bit SIPO synchronous shift register in a timing waveform. Correctly indicate the clock, input and output sequences when the shift pulse is applied. [**2 marks**]