THE PAPUA NEW GUINEA UNIVERSITY OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND COMMUNICATIONS ENGINEERING

SECOND SEMESTER EXAMINATION (2023)

EE221 DIGITAL LOGIC SYSTEMS

BEEL2, BEBE2 and BSAP2

TIME ALLOWED: 3 HOURS

INFORMATIONS FOR STUDENTS

1. You have **TEN [10] MINUTES** to read through the paper. You must not begin writing during this time.
2. Answer **FIVE QUESTIONS**. Attend to all the Examination Questions **in any order**. Total marks available is 100 marks.
3. All Answers must be written in the **ANSWER BOOK** supplied.
4. The final two pages of the Exam Paper containing graphs will be removed and placed in your answer sheets.
5. **COMPLETE THE DETAILS REQUIRED ON THE FRONT COVER OF YOUR ANSWERBOOK – DO THIS NOW.**
6. Only the drawing instruments and the calculators are permitted on your desk. Text books and notebooks are **NOT** permitted.
7. If you are found cheating in the Examination, the penalties specified by the University shall apply.
8. **TURN OFF** all **Mobile Phones** and place them on the floor under your seat before the start of Examination.

QUESTION ONE [20 Marks]

Verify each statement and write true or false as your answer in the answer booklet.

(a) Negation does not require the use of 2's complement process.
(b) For a particular Boolean expression, the alphabets represent input and out variables while the operator represent the logic gate.
(c) Truth table summarizes the results of all possible combinations of all the logical inputs.
(d) Binary number is a positional value system.
(e) XOR gate and NOR gate are universal gates since they can be used to implement other logic gates.
(f) Data value hexadecimal A45 is a positive number if it is a signed number.
(g) Data value hexadecimal 745 is a positive number if it is a signed number.
(h) ASCII is an 8 bit binary code for alphanumeric characters.
(i) ASCII can be used to represent a total of 128 alphanumeric characters.
(j) If the ASCII data 11000011 is transmitted then even parity for error detection is used.
(k) Even and Odd parity method of error detection is only used to detect two bit error.
(l) A microprocessor unit with 16 Bit address bus from A0 to A15 will have address range from 0000 0000 0000 0000 to 1111 1111 1111 1111.
(m) The least significant carry input (C0) of a full adder circuit is set to 0 when 2's complement addition is performed.
(n) Multiplexer is sometimes referred to as data distributor.
(o) An even bit generator will produce logical value 1 if the total number of ones transmitted is even.
(p) An odd bit generator will produce logical value 0 if the total number of ones transmitted is odd.
(q) A shift register counter has shift register circuit structure and a feedback link from the output of the last FF to the data input of the first FF.
(r) There are two types of ripple counters. One is ring counter and the other is Johnson counter.
(s) Clocked SC Flip-Flop cannot be used in practical applications due to ambiguity associated with conditions S = C = 1.
(t) Asynchronous inputs in clocked Flip-Flops can be utilized to override the operations determined synchronous inputs.

QUESTION TWO [20 Marks]

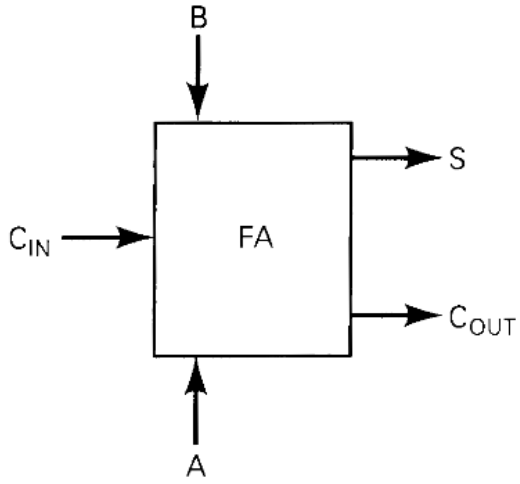
(a) Apply De-Morgans theorems to simplify the Boolean expression below and draw the simplified logic ciruit. [6 marks]

$$x = \overline{\overline{\overline{A}\overline{B}CD}} + \overline{A + \overline{B}}$$

(b) Truth table given in **Figure1** (a) belongs to a full adder circuit. Perform the following tasks. [14 marks]

Augend bit input	Addend bit input	Carry bit input	Sum bit output	Carry bit output
A	B	C_{IN}	S	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a)



(b)

Figure 1: (a) Truth Table and (B) Block Diagram for Full Adder

(i) Form the appropriate expressions for the sum output (S) in sum of product (SOP) form, and simplify.

(ii) Form the appropriate expressions for the carry output (Cout) in sum of product (SOP) form, and simplify.

(iii) Draw the logic circuit diagram of the full adder circuit.

QUESTION THREE [20 Marks]

Perform analysis and design of the following combinational logic circuit. Error detection in information transmission involves determining whether one of the bits contained in the transmitted data is lost or intact. Even and odd parity methods of single bit error detection are commonly used. Design an even bit generator and error detector circuit for 4-bit data transmission system by fulfilling the following design steps.

(a) Establish the truth table for the detection of "the need for even parity generation". [6 marks]

(b) Writer down the Boolean expression by summing up the product terms corresponding to output logic 1 in your truth table in **(a)**. [2 marks]

(c) Simplify the Boolean expression formed in (b) and convert to an appropriate form. Use XOR and XNOR Boolean operators where applicable. [4 marks]

(d) Draw the logic circuit of the even bit generator from the expression formed in **(b)** and simplified in **(c)**. [3 marks]

(e) Draw the logic circuit diagram of an even bit error checker. [5 marks]

QUESTION FOUR [20 Marks]

(a) The MOD16 asynchronous counter is provided in **Figure 2**. [9 marks]

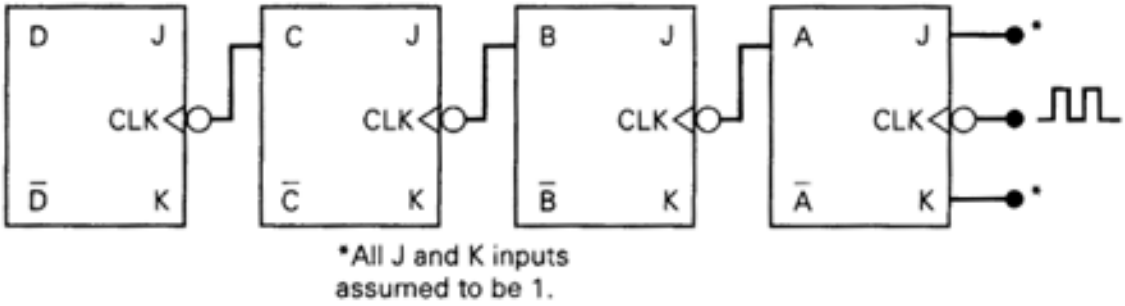


Figure 2: MOD 16 Asynchronous Counter

(i) Based on the circuit provided in **Figure 2** draw the transition state diagram of a ripple (asynchronous) counter that will count from 1000 to 1110 and recycle.

(ii) Draw the logic circuit diagram of a ripple (asynchronous) counter that will count from 1000 to 1110 and recycle. Use JK flip-flops and NAND gates in your diagram.

(b) Perform the following taks relating to Johnson Counter. [11 marks]

(i) Draw the logic circuit diagram of a MOD6 Johnson counter.

(ii) If the MOD6 johnson counter has six states and the initial state is 000, determine the states based on the circuit you have drawn above by duplicating the table below in your answersheet and filling it out.

Count Step	Binary Output Code
0	000
1	
2	
3	
4	
5	

(iii) Draw the decoding circuit for Count Step = 4.

QUESTION FIVE [20 Marks]

Draw the waveforms in parts **(a)**, **(b)** and **(c)** based on your knowledge of the logic circuits associated with the truth tables shown in **Figure 3**.

Tear out the pages containing waveforms and insert in the center of your exam answer booklet.

D	CLK	Q
0	↑	0
1	↑	1

(a)

$\overline{\text{PRESET}}$	$\overline{\text{CLEAR}}$	FF response
1	1	Clocked operation*
0	1	Q = 1 (regardless of CLK)
1	0	Q = 0 (regardless of CLK)
0	0	Not used

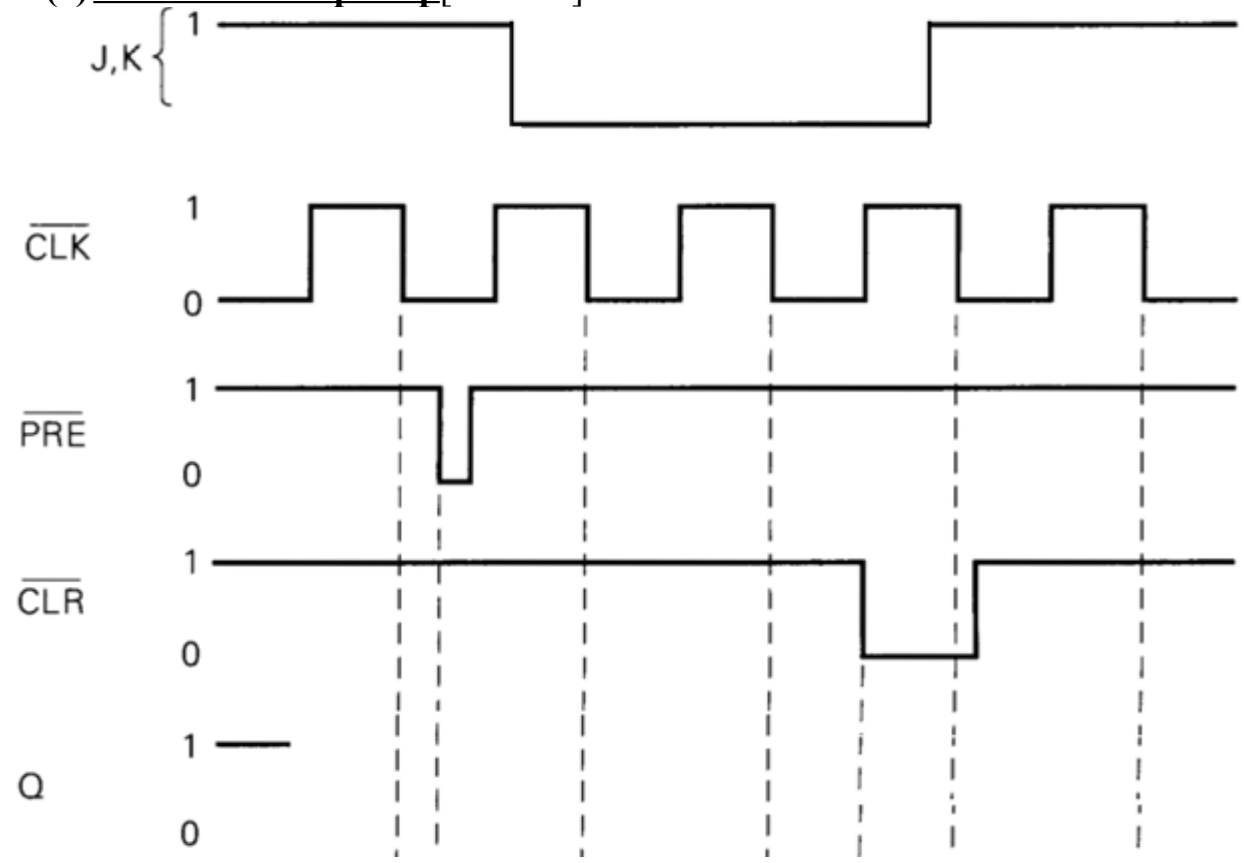
*Q will respond to J, K, and CLK

(b)

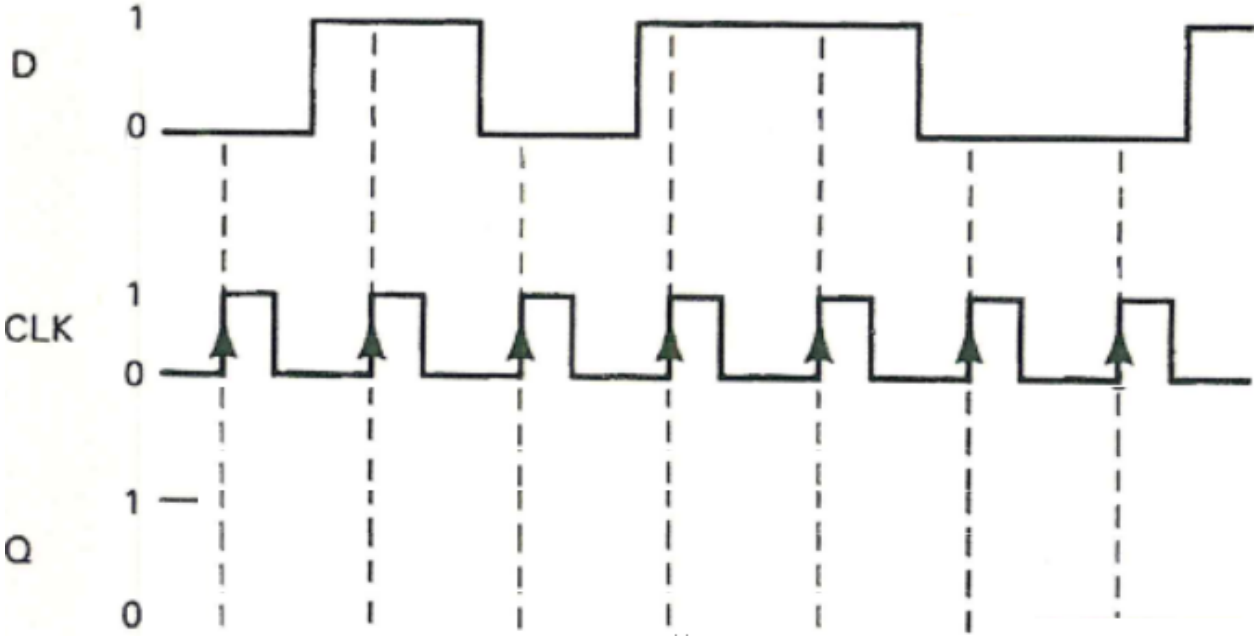
Figure 3: Truth tables for (a) Clocked D Flip-Flop and (b) Clocked JK Flip-Flop

Name: _____ **ID No.:** _____

(a) <u>Clocked JK Flip-Flop</u>[6 marks]



(b) <u>Clocked D Flip-Flop</u> [6 marks]



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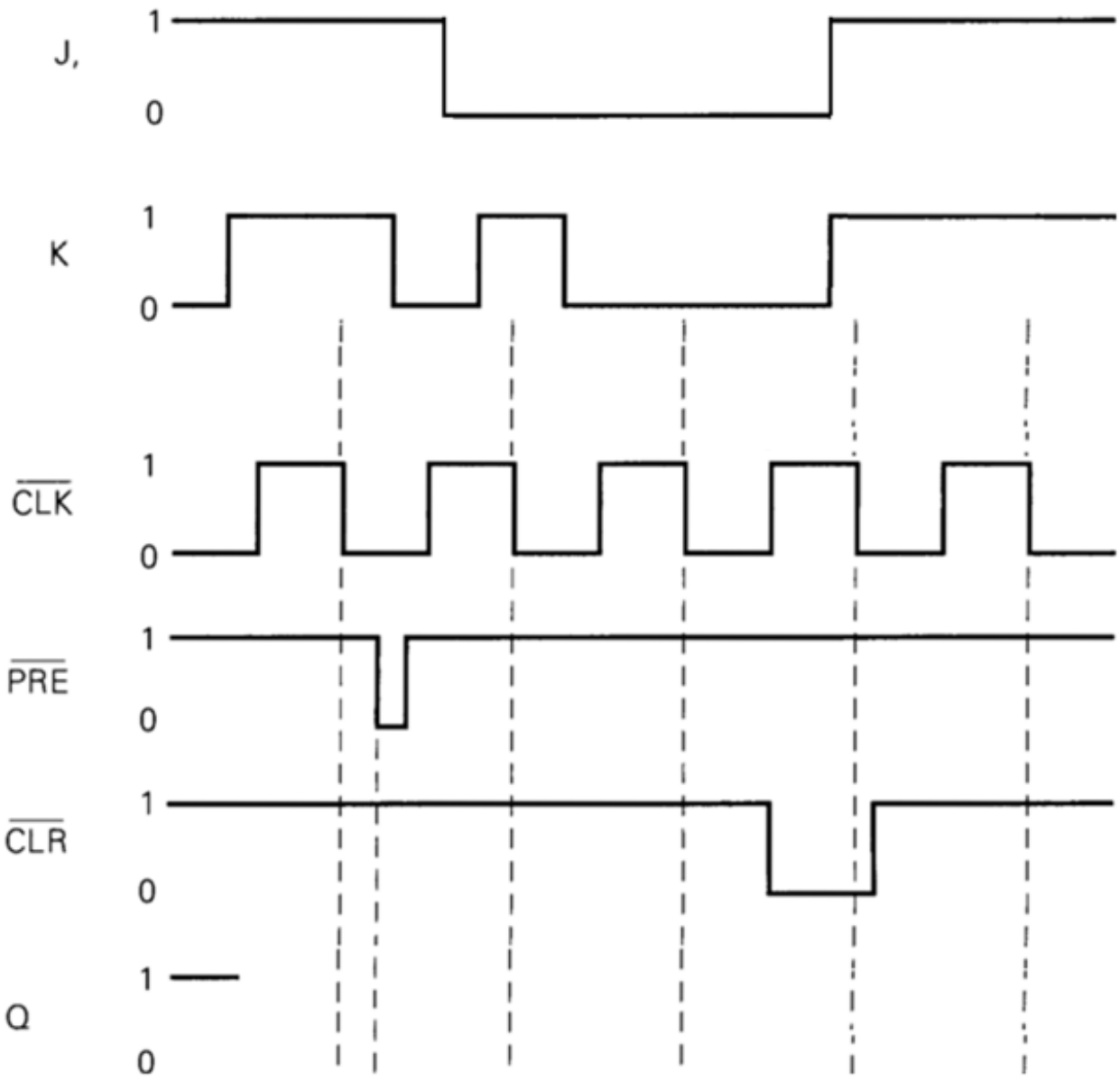
(c) <u>Clocked JK Flip-Flop with Asynchronous Inputs</u> [8 marks]



FINAL PAGE OF EXAMINATION QUESTION