THE PAPUA NEW GUINEA UNIVERSITY OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND COMMUNICATIONS ENGINEERING

FIRST SEMESTER EXAMINATION – 2022

EE415: POWER ELECTRONICS I

BEEP4

TIME ALLOWED: 3 HOURS,

INFORMATIONS FOR STUDENTS

1. You have **TEN [10] MINUTES** to read through the paper. You must not begin writing during this time.
2. Answer **FIVE QUESTIONS**. Attend to all the Examination Questions **in any order**.
3. All Answers must be written in the **ANSWER BOOK** supplied.
4. Make sure that you have a **DATA** and **SUPPLEMENT FORMULA sheets** at page 8 and page 9 of the Exam Paper.
5. **COMPLETE THE DETAILS REQUIRED ON THE FRONT COVER OF YOUR ANSWERBOOK – DO THIS NOW.**
6. Only the drawing instruments and the calculators are permitted on your desk. Text books and notebooks are **NOT** permitted.
7. If you are found cheating in the Examination, the penalties specified by the University shall apply.
8. **TURN OFF** all **Mobile Phones** and place them on the floor under your seat before the start of Examination.

QUESTION1 [20 Marks]

Question 1 has two parts to it, **(a)**, and **(b)**. Part (a) is true or false statements, part and (b) requires sketches and some analytical work.

(a) Attend to the following **TRUE OR FALSE** statements and answer them. Write on your answer sheet **True** if the statement is true or **False** if you think otherwise.

(i) In forward blocking operation, middle junction (J2) of the thyristor is reversed bias.

(ii) Depletion type power MOSFETS have physical channel.

(**iii**) When anode terminal of a thyristor is connected to negative source with respect to cathode, junction1 and junction3 are in reverse bias.

(iv) For enhancement type power MOSFET to start conducting, source to gate voltage (V_{GS}) must be greater than or equal to the threshold voltage (Vth).

(v) Input Capacitance (C_{iss}) of a power MOSFET is contributed from gate to source capacitance (C_{GS}), and gate to drain capacitance (C_{GD}).

(vi) Turn on time comprise of rise time and fall time (ton = tr + tf).

(vii) Gate drive circuits can be isolated from digital electronics by the use of either opto-coupling or transformer coupling.

(viii) Turn off delay time (t_{doff}) is time taken for overdrive voltage to fall to pinch-off voltage.

(ix) Current flow between the gate to drain of a power MOSFET is significantly large during conduction time.

(x) Enhancement type power MOSFET operates on the basis of capacitive induction.

(b). PWM inverter can be broadly classified into single or three phase DC-AC power converters. Each type of PWM inverter has unique topology. Attend to the following instructions relating to DC-AC converters and provide correct answers accordingly.

(i) Provide a sketch for a half-bridge PWM inverter topology. The inverter consists of “totem pole” gate drive circuit and two power MOSFETs are employed to perform power switching. The DC source of VS/2 is supplied to obtain a AC power output.

(ii) Provide sketch for the output voltage over one cycle.

(iii) Express the instantaneous out voltage of half-bridge PWM inverter as a Fourier expansion expression.

(iv) If the inverter feeds a RL load, provide expression for the instantaneous load current. Provide also the general expression of the harmonic load angle.

QUESTION2 [20 Marks]

Attend to question parts **(a)** and **(b)** based on information provided. Part **(b)** is based on **figure1**.

(a) A drive IC used to operate a Power MOSFET switching circuit. It is capable of sinking and sourcing 1A is used to drive a MOSFET switch which has the following, C_{GS} = 1000pF; C_{DS} = 200pF; and V_{th} = 4V.
(i) Find the value of R_g such that V_{GS} on turn-on reaches 15V within 500 ns.
(ii) Calculate turn on time for the power MOSFET switching circuit.
(iii) Calculate rise time for the drive circuit.
(iv) If pinch-off voltage of 9Volts is reached during discharging, find the turn off delay time tdoff.
(v) Calculate the fall time (t_f).
(vi) Calculate maximum design frequency of PWM signal if turn on time requirement for switching is 1% of the switching period.

(b) Attend to the following analysis, paying attention to details provided with respect to **figure1**. The buck-boost regulator in **figure1** has an input voltage of *Vs* = 15 V. The duty cycle is *k* = 0.45 and the switching frequency is 35 kHz. The inductance is *L* = 150 µH and filter capacitance *C* = 220 µF. The average load current is I_a = 2.5 A.

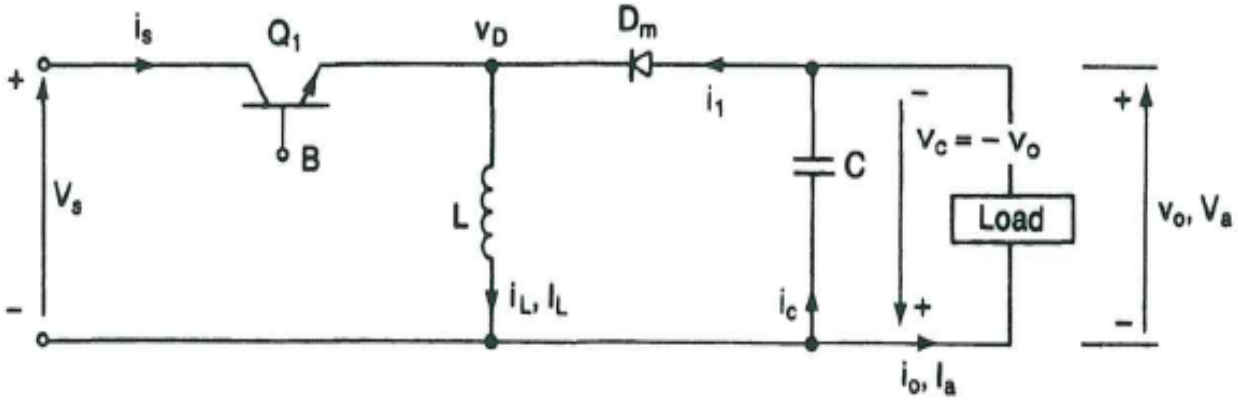

Figure1: Buck-Boost Regulator **(Question2b)**

Determine;
(i) the average output voltage, V_a;
(ii) the peak-to-peak output voltage ripple, ΔV_c;
(ii) the peak-to-peak ripple current of the inductor, ΔI; and
(iv) the peak current of the transistor, I_p.

QUESTION3 [20 Marks]

Thyristors are fabricatred using **pnpn** structured extrinsic semiconductor devices. Thyristor schematic provided in **figure 2 (a)** has a doping profile provided in (b). The doping profile is constructed along the dotted line AB indicated in (a). The p-type and n-type semiconductor devices have ideal carrier concentration to suit thyristor difussion profile provided in **figure 2**. For this design, the concentration of **p-type1** is 2.5 x 10^{20} cm^{-3}, **n-type1** is 3.5 x 10^{14} cm^{-3}, **p-type2** is 3.5 x 10^{17} cm^{-3} and **n-type2** 1.5 x 10^{21} cm^{-3}. **Note**; n-type1 is located at the Anode.

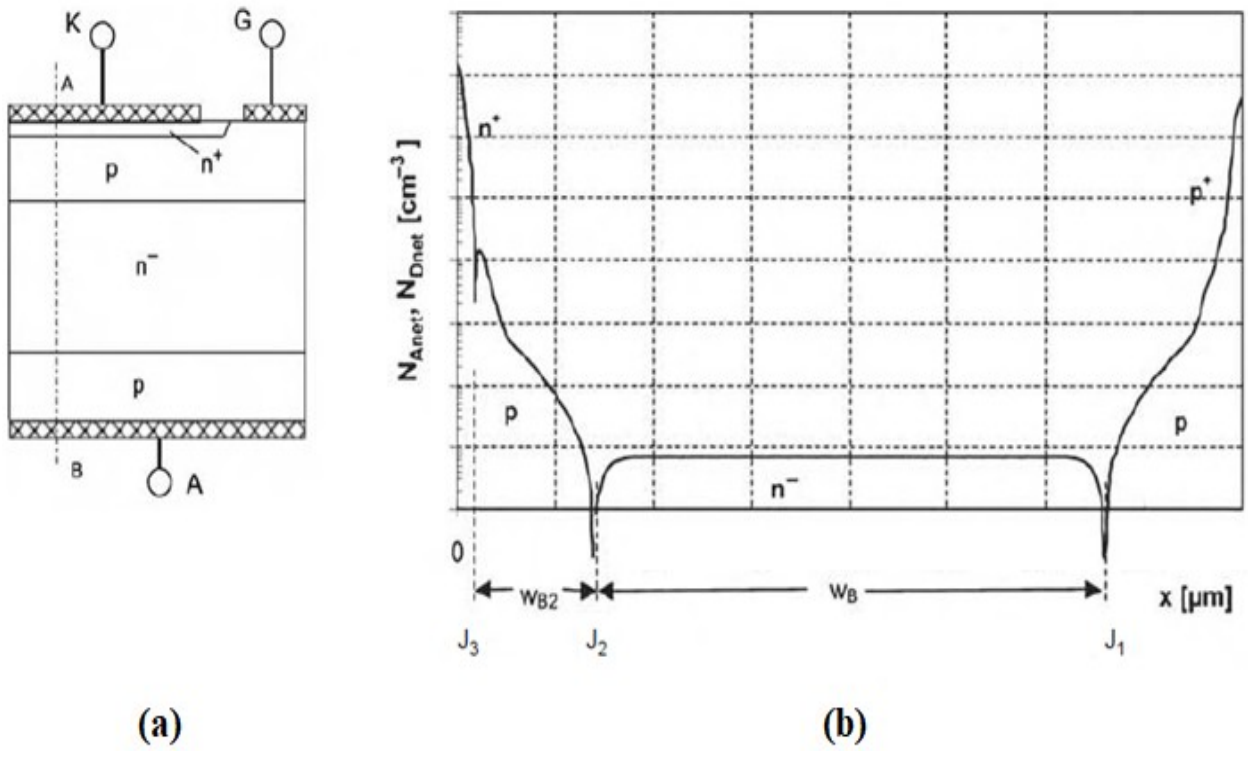

Figure2: Thyristor Diffusion profile for **(Question3)**

Lets say that the thyristor is made from silicon (Si) material, which has electron mobility (μ_n) at RT is 1400 $cm^2 V^{-1}s^{-1}$; μ_n/μ_p = 3.1; the intrinsic concentration is n_i = $1.05 \times 1.5 \times 10^{15}$ cm^{-3}, and relative permittivity of silicon is ε_{rSi} = 11.9; (note that ε_{si} = ε_{rSi}). At room temperature (300K), the acceptor and donor concentrations of the p-types and n-types are shown on the profile. ***Note:*** For this doping profile, junction-J1 is the first junction from the Anode (A); junction-J2 is the middle junction, while junction-J3 is final junction towards the Cathode (K).

Perform the following analysis from **(a)** to **(d)** on the Thyristor based on the information provided above.

(a) Sketch the thyristor schematic diagram and indicate the alignment of charge carriers along the three junctions.
(b) Identify majority and minority carriers in each p-type and n-type material used and calculate the values for majority and minority carriers. P-type material1 is from anode PNPN. Take note that when selecting majority carriers densities from the graph, use the highest values.
(i) P-type Material-1
(ii) N-type Material-1
(iii) P-type Material-2
(iv) N-type Material-2

(c) Calculate build-in voltage (V_B) established across the space charge of each junction.
(i) build-in voltage (V_{B1}) established across junction1
(ii) build-in voltage (V_{B2}) established across junction2
(iii) build-in voltage (V_{B3}) established across junction3

(d) Estimate by calculation, the Forward Breakover Voltage V_{BO} of the thyristor. If the spacecharge of junction j2 occuplies W_{BJ} = 2.943 x 10^{-4} cm. Use heavily doped concentrations of the junctions N_A or N_D whichever applicable as calculated in **(b)**.

QUESTION4 [20 Marks]

Analysis for this question are based on ac-dc converter topology given in **figure3**. The single-phase full converter of **figure3** has Resistive load having R = 1.5 Ω. The input voltage is Vs = 120 V at (rms) 60 Hz, the thyristor is triggered at α = 60°.

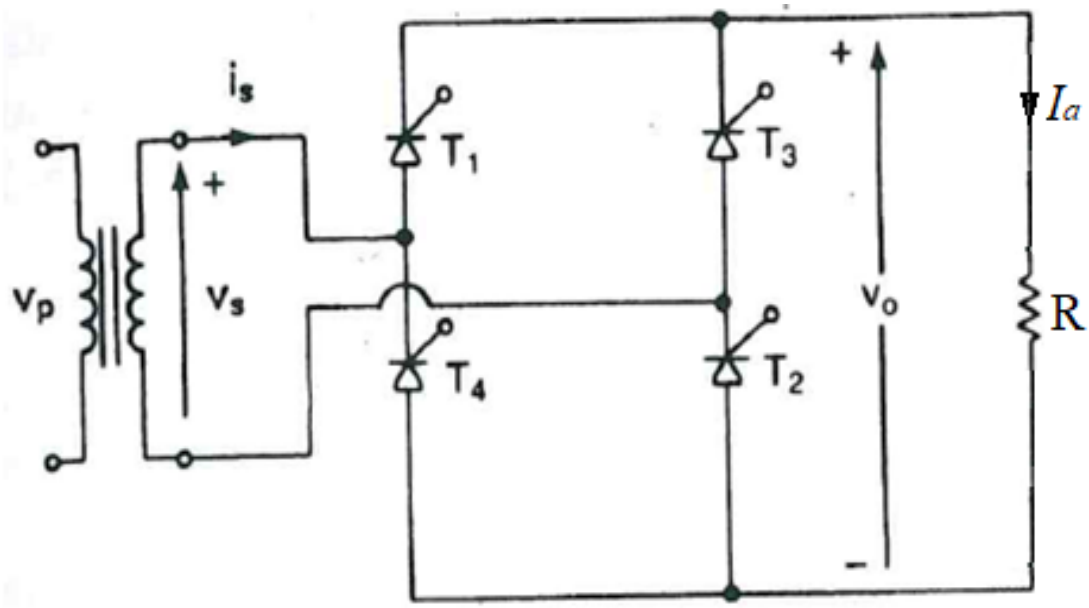

Figure3: Single-phase AC-DC converter **(Question4)**.

Determine;
(a) the load current I_a
(b) the average thyristor current, I_A;
(c) the rms thyristor current, I_R;
(d) the rms output current, I_{rms};
(f) the rms value of the fundamental component of the input current, I_{S1};
(g) the rms value of the input current to 9th Order Harmonic, I_S;
(h) the Total Harmonic Factor, *THF*;

<u>QUESTION5 [20 Marks]</u>

The three-phase bridge rectifier shown in **figure 4** has an RL load, E = 12V and is supplied froma wye-connected supply. The load comprise of L = 3.5 mH inductor, and resistor of R = 5 Ω. The line-to-line voltage is V_{ab} = 208 V, at supply frequency of 50 Hz.

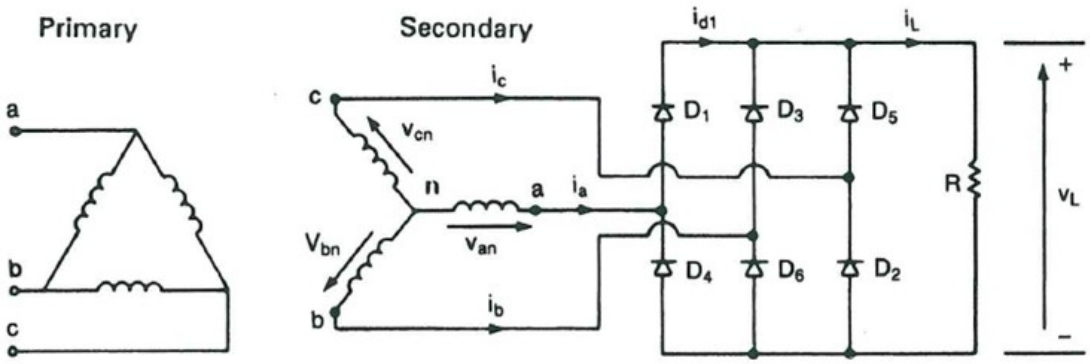

Figure4: Three-Phase wye-connected Diode Rectifier **(Question5)**.

Perform the following analysis based on the information given above and relating to 3 phase diode rectifier given in **figure4**.

Calculate;
(a) the steady state load current, I_1 at ***wt* = 50°**;
(b) the average diode current, I_d;
(c) the rms diode current, I_r;
(d) the rms output current, I_{rms};
(e) the efficiency of conversion for the three phase power rectifier, μ.

FINAL PAGE OF EXAMINATION QUESTION

General Formula and Data Sheet

Following are some formullas that may be useful in some parts of calculations for certain questions. It is part of knowledge test in this exam that the canditate be able to find the unlabelled formula meaningful in appropriate questions.

(1) Formula 1

$$i_L = \frac{\sqrt{2}\,V_{ab}}{Z}\left[\sin(\omega t - \theta) + \frac{\sin(2\pi/3 - \theta) - \sin(\pi/3 - \theta)}{1 - e^{-(R/L)(\pi/\omega)}}\, e^{-(R/L)t}\right] - \frac{E}{R}$$

(2) Formula 2

$$I_1 = \frac{\sqrt{2}\,V_{ab}}{Z}\,\frac{\sin(2\pi/3 - \theta) - \sin(\pi/3 - \theta)e^{-(R/L)(\pi/3\omega)}}{1 - e^{-(R/L)(\pi/3\omega)}} - \frac{E}{R}$$

(3) Formula 3

$$V_{\text{dc}} = \frac{2}{2\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin\omega t\, d(\omega t) = \frac{2V_m}{2\pi}\left[-\cos\omega t\right]_{\alpha}^{\pi+\alpha}$$

$$= \frac{2V_m}{\pi}\cos\alpha$$

(4) Formula 4

$$I_s = \left(\sum_{n=1,2,\ldots}^{\infty} I_{sn}\right)^{1/2}$$

where

$$I_{sn} = \frac{1}{\sqrt{2}}(a_n^2 + b_n^2)^{1/2} = \frac{2\sqrt{2}\,I_a}{n\pi}\cos\frac{n\alpha}{2}$$

(5) Data Sheet

Symbol	Value	Description
q	1.602×10^{-19} coulomb	electronic charge
q	1.602 × 10-19	conversion from joules to eV
m_0	9.108×10^{-31} kg	electron rest mass
c	2.99792458×10^{8} m/s	speed of light in vacuum
ε_0	8.85418×10^{-14} farad/cm 8.85418×10^{-12} farad/m	permittivity of free space
h	$6.62606957 \times 10^{-27}$ erg·s $6.62606957 \times 10^{-34}$ joule·s	Planck's constant
k	$1.3806488 \times 10^{-16}$ erg/K $1.3806488 \times 10^{-23}$ joule/K	Boltzmann's constant
σ	5.67×10^{-8} J/m^{2}s K^4	Stefan-Boltzmann constant
kT/q	0.02586 V	thermal voltage at 300 K
λ_0	wavelength of 1 eV photon	1.24 μm