THE PAPUA NEW GUINEA UNIVERSITY OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMMUNICATIONS ENGINEERING

SECOND SEMESTER EXAMINATION (2023)

EE222 ANALOG ELECTRONICS AND CIRCUITS

TIME ALLOWED: 3 HOURS

INFORMATION FOR STUDENTS

1. You have **TEN (10) MINUTES** to read the paper. You must not begin writing during this time.
2. All answers must be written in the **ANSWER BOOK** supplied.
3. **COMPLETE THE DETAILS REQUIRED ON THE FRONT COVER OF YOUR ANSWER BOOK - DO THIS NOW**.
4. Only drawing instruments and calculators are permitted on your desk.
5. Answer all questions.
6. Total available mark is 50.
7. If you are found cheating in the Examination, the penalties specified by the University shall apply.
8. **TURN OFF** all mobile phone and place them on the floor under your seat before the start of examination.

QUESTION ONE [4 + 2+ 4 = 10 Marks]

a. Define diode and explain in terms of forward and reverse bias. **(4 Marks)**

b. Calculate the intrinsic carrier concentration in Germanium at T = 300 K. Refer to the table provided in Figure 1. **(2 Marks)**

Semiconductor constants

Material	Eg (eV)	B ($cm^{-3}\ K^{-3/2}$)
Silicon (Si)	1.1	5.23×10^{15}
Gallium arsenide (GaAs)	1.4	2.10×10^{14}
Germanium (Ge)	0.66	1.66×10^{15}

Figure 1: Semiconductor Material Constants

a. Refer to the table in Figure 1, calculate the thermal equilibrium of electron and whole concentrations for:
   I. If germanium if doped with phosphorous at the concentration of $N_d = 10^{18} cm^{-3}$. **(2 Marks)**
   II. If Germanium is doped with Boron at the concentration of $N_a = 5 \times 10^{18} cm^{-3}$. **(2 Marks)**

QUESTION TWO [3 + 3 + 4 = 10 Marks]

a. Draw the process in which P-Type and N-Type are created to form PN Junctions diode. **(3 Marks)**
b. Draw and indicate diffusion and drift of holes and electrons when pn junction diode is formed**. (3 Marks)**
c. Assume both D1 and D2 are silicon diode, calculate V_0 and I_0 from the PN Junction diode circuit in Figure 2 below. **(4 Marks)**

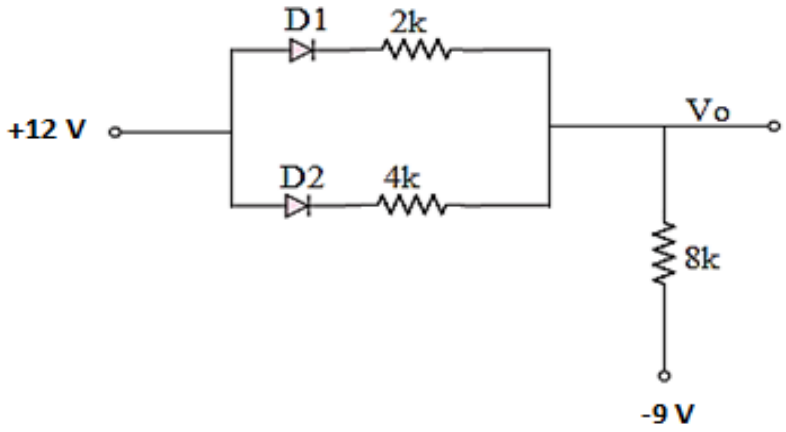

Figure 2: PN Junction Diode Circuit

QUESTION THREE [4 + 6 = 10 MARKS]

a. Calculate the characteristics ($I_B, I_C, I_E, \wedge V_{CE}$¿ of a circuit containing an emitter resistor for the circuit in Figure 3. Let $V_{be(on)}=0.7$ and $\beta=75$. Note that the circuit has both positive and negative power supply voltages. **(4 Marks)**

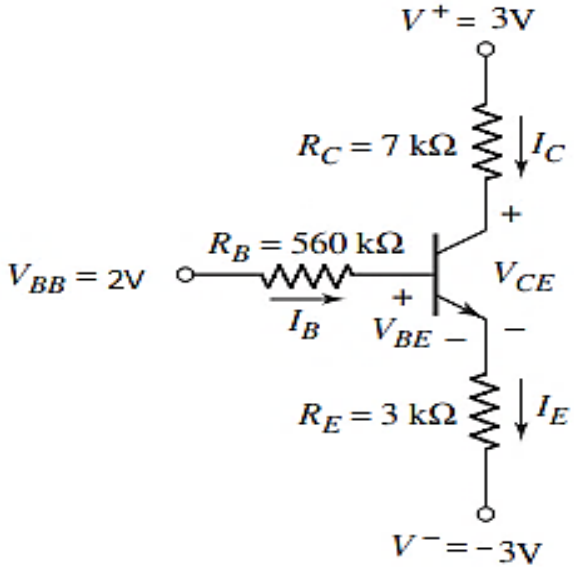

Figure 3: Transistor Circuit Containing an Emitter Resistor

b. Calculate the characteristics ($I_B, I_C, I_E, V_o, I_1, I_L \wedge V_{CE}$¿ of a npn bipolar transistor circuit with a load resistance. The load resistance can represent a second transistor stage connected to the output of a transistor circuit. The transistor parameters are $V_{BE(on)}=0.7V$, $\beta=100$ **(6 Marks)**

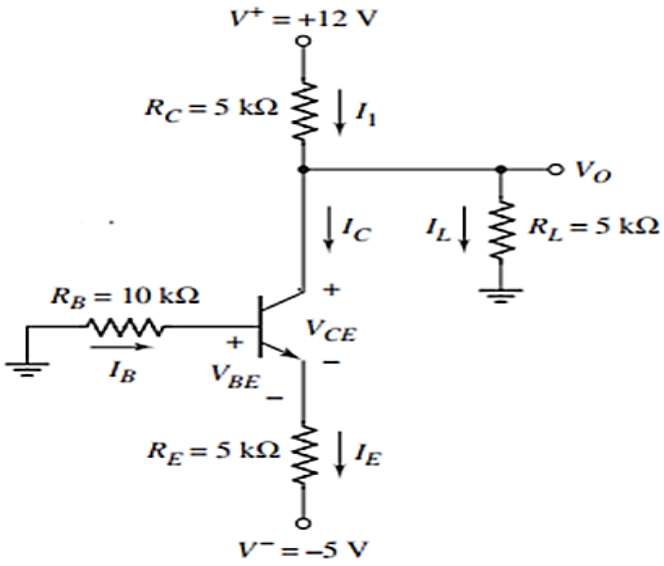

Figure 4: npn Bipolar Transistor Circuit

QUESTION FOUR [6 + 4 = 10 MARKS]

a. From the circuit in Figure 5, do DC load Analysis with a load line and small signal AC load analysis. **(6 MARKS)**

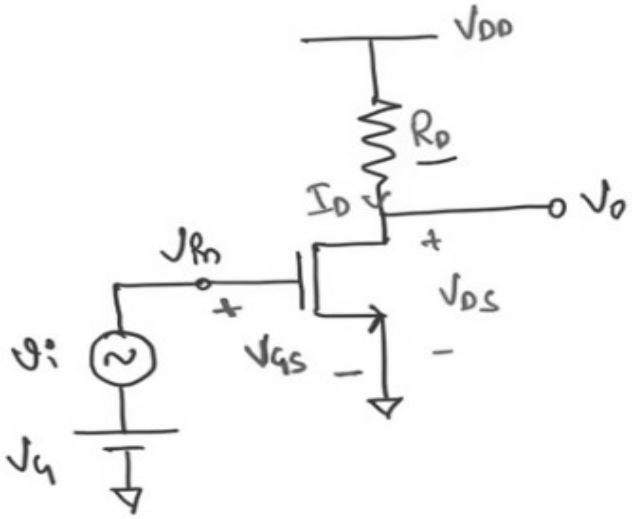

Figure 5: MOSFET Circuit Analysis

b. Calculate I_D and determine if it is in saturation region. Take $V_{TN}=2.0\,V$ and $k=0.4\,mA/V^2$. **(4 MARKS)**

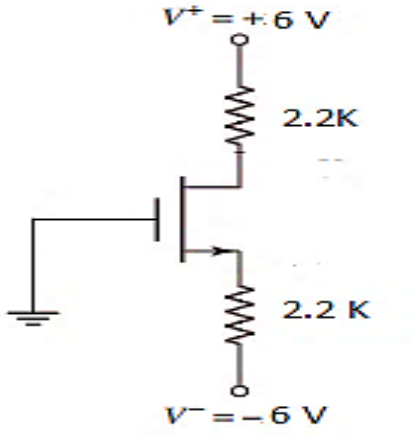

Figure 6: MOSFET Circuit Calculation

QUESTION FIVE (10 MARKS)

Calculate the drain current and source-to-drain voltage of a common source circuit with a p-channel enhancement-mode MOSFET. Consider the circuit shown in Figure 7 assuming that $R_1 = R_2 = 50\,k\Omega$, $V_{DD} = 5\,V$, $R_D = 7.5\,k\Omega$, $V_{TP} = -0.8\,V$, $K_p = 0.2\,mA/V^2$.

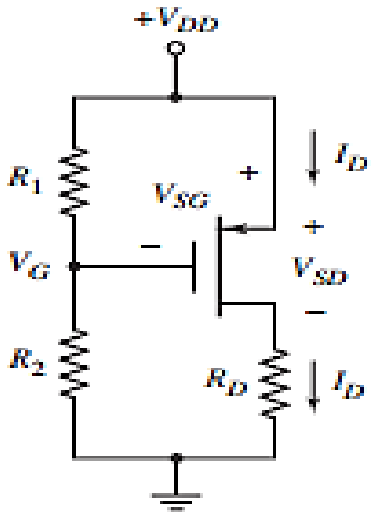

Figure 7: p-channel Enhancement-mode MOSFET