THE PNG UNIVERSITY OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL & COMMUNICATIONS ENGINEERING DEPARTMENT

SECOND (2^{ND}) SEMESTER (2021)

EN123-Introduction to Circuits and Electronics

TIME ALLOWED: 3 HOURS

INFORMATION FOR STUDENTS:

1. You have **TEN (10) MINUTES** to read this paper. Do not write during this allocated time

2.There are **Five (5) Questions** in this Exam Booklet. **Answer ALL Questions.**

3.All answers must be written in the **Answer Booklet**

4.COMPLETE STUDENT DETAILS ARE TO BE FILLED ON THE ANSWER BOOKLET-DO THIS NOW

5.Only drawing instruments and calculators are allowed on your desk. Textbooks and notebooks are **NOT** allowed

6.If you are found **Cheating** in this Exam, penalties specified by the **University** shall be applied.

7.TURN OFF all your mobile phones and place them on the floor under your seat before you start the examination

QUESTION 1

Fill in the blanks with the most appropriate word

a) _____ is a close path where electrons flow.

b) ___ is the potential difference between positive and the negative end of the resistor.

c) In a waveform, the ____ give the strength of the wave.

d) When electrons come out to play, their speed is the inverse of _____.

e) Resistors are used to _____ current, divide voltages, and pull-up I/O lines.

f) Lumped elements meet at the ___.

g) The path between two nodes defines a _____.

h) Current flowing within a section of the circuit form a ____.

i) Voltage required in a diode to conduct current between the PN junction is known as the _____.

j) The NPN transistor is a sandwich of two _____ type diodes.

[Total 20 Marks]

QUESTION 2

(a) Three resistors of resistances 10 Ω, 20 Ω and 15 Ω are connected in parallel across a 50 V supply.

(i) Determine the currents in each resistor and the total current from the supply.

(ii) If the 20 Ω resistor becomes disconnected, recalculate the currents. Using the results, discuss why the parallel connection is commonly used in electric connections inside a house.

(iii) With all three resistors connected, a fourth 5 Ω resistor is connected in parallel to the other three resistors. Calculate the currents through the four resistors and the total current from the supply. Using the results, discuss why it is dangerous to connect additional loads to a wired system, for which the system has not been designed to carry.

[09 Marks]

(b) Given the full wave bridge rectifier circuit shown in Figure 1.

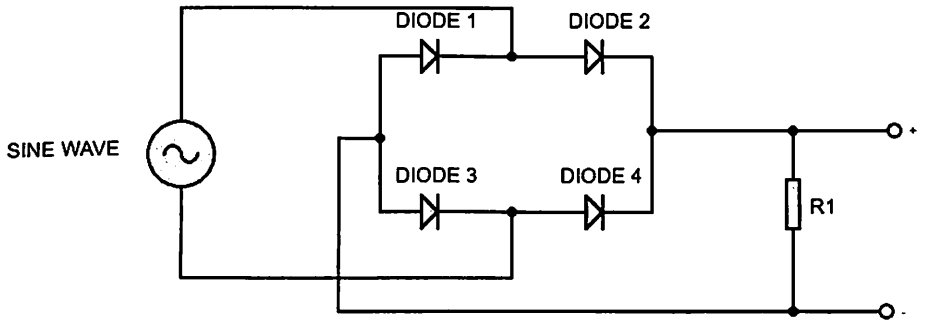

Figure 1

Describe the operation of the full wave bridge rectifier with suitable input and output waveforms.

[06 Marks]

(c) Consider the circuit shown in Figure 2, of a transistor used as a switch.

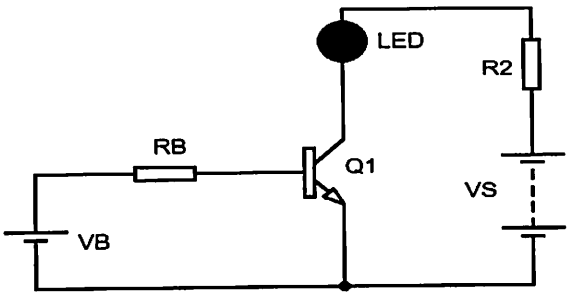

Figure 2

Given that Vs = 3V, VBE = 0.3V, IC = 9 mA, and R1 = 1kΩ, calculate the base current IB of Q1 using KVL. Find the current gain (ß) of the transistor Q1.

[05 Marks]

[TOTAL 20 Marks]

QUESTION 3

(a) Given in Figure 3 is the circuit diagram for a 2 to 4 Binary Decoder. Determine the truth table for the 2 to 4 Decoder.

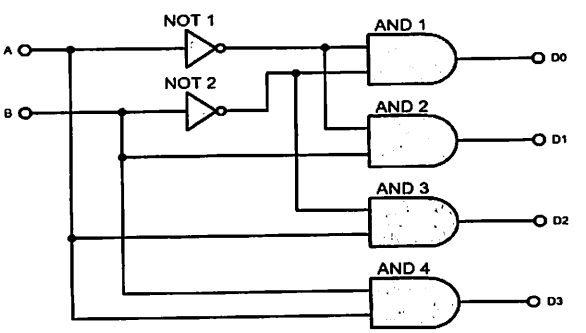

Figure 3.

[04 Marks]

(b) Consider the Darlington transistor pair shown in Figure 4.

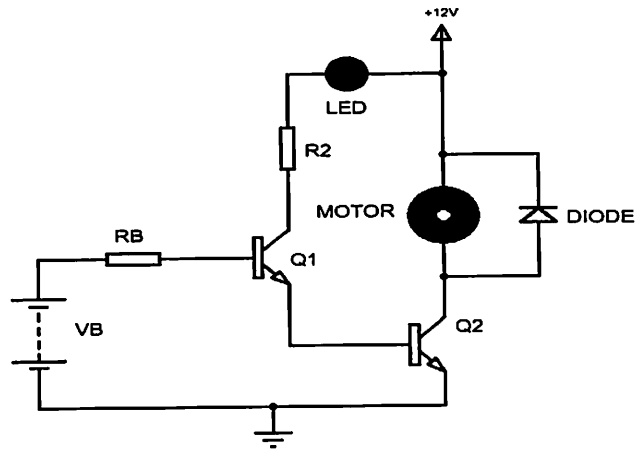

Figure 4.

The Darlington transistor pair is used to switch two loads, an LED and a DC motor. When the transistors are switched on, the two loads are fully connected. Given the current into the base of transistor Q1, I_{B1} = 4.8 mA, and gain for both transistors is $\beta = 80$. Determine the emitter current I_{B2} for transistor Q1. Also calculate the emitter current I_{E2} of transistor Q2 for the Darlington transistor pair.
Compare the emitter currents of Q1 and Q2 and discuss how the Darlington pair is useful in driving two different kinds of industrial loads.

[12 marks]

(c) Consider the half-wave bride rectifier shown in Figure 5

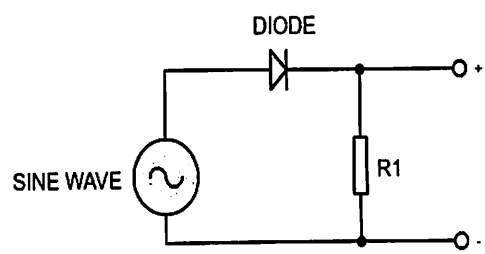

Figure 5

With suitable input and output waveforms, describe the operation of the circuit shown in Figure 5.

[04 Marks]

[TOTAL 20 Marks]

Question 4

A) (i) Add −118 and −32 firstly using eight-bit 2's complement arithmetic and then using 16-bit 2's complement arithmetic.
(ii) Comment on the results.

[8 Marks]

B) (i) Add (0011 0101 0110)BCD and (0101 0111 1001)BCD using the excess-3 addition method
(ii) Verify the result using equivalent decimal addition.

[8 Marks]

C) How would you hardware-implement a four-input OR gate using two-input OR gates only?

[4 Marks]

[Total 20 Marks]

QUESTION 5

A) The data sheet of a quad two-input NAND gate specifies the following parameters: IOH(max.)=0.4
mA, VOH(min.)=2.7 V, VIH (min.)=2V, VIL(max.)=0.8 V, VOL(max.)=0.4 V, IOL(max.)=8 mA,
IIL(max.)=0.4 mA, IIH (max.)=20x10-6A, ICCH(max.)=1.6 mA, ICCL(max.)=4.4 mA, tpLH =tpHL=15 ns and a supply voltage range of 5 V. Determine

(i) the average power dissipation of a single NAND gate,
(ii) the maximum average propagation delay of a single gate,
(iii) the HIGH-state noise margin
(iv) the LOW-state noise margin

[12 Marks]

B) Refer to Question 5 (A). How many NAND gate inputs can be driven from the output of a NAND gate of this type?

[4 Marks]

C) A certain TTL gate has IIH=20x10-6A, IIL=0.1 mA, IOH=0.4 mA and IOL=4 mA. Determine the input and output loading in the HIGH and LOW states in terms of UL.

[4 Marks]

[Total 20 Marks]